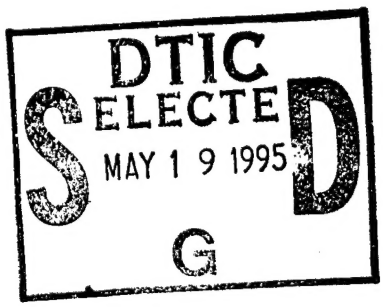
Complementary 2-D MESFET for Low Power Electronics

Interim Report # 1

Air Force SBIR Phase I
Contract Number: F33615-95-C-1679

May 16, 1995



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(AirForce SBIR Contract F33615-95-C-1679)

Phase I Interim Report #1

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes the progress in each task area since during the period 2 MAY 95 - 16 MAY 95.

Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. A preliminary heterostructure design using AlGaAs/InGaAs/GaAs material system has been worked out and a quote for the material growth and analysis is being negotiated. A second structure of p-type GaAs is also being considered for basic ohmic and Schottky contact evaluations. Finally, the prospective use of ion-implantation for ohmic contacts is being investigated. A subcontract to the University of Virginia Department of Electrical Engineering is being negotiated for part of the fabrication tasks.

Task 2: Development of p-Channel 2-D MESFET Model

The initial development of a p-channel 2-D MESFET model is also underway. Our preliminary approach will be to modify the n-channel model to use p-type material parameters including the hole mobility and saturation velocity, Schottky barrier height, and larger series resistance terms.

Task 3: Complementary 2-D MESFET Circuit Simulations

Circuit simulations of complementary 2-D MESFET circuits will take place later in the Phase I project.

Task 4: Manufacturability and Technology Insertion Issues

A comprehensive technology analysis of complementary 2-D MESFET circuits will be performed throughout the duration of the Phase I project. It will serve to summarize the main advantages of a complementary 2-D MESFET over existing technologies and to address any potential barriers to insertion of the complementary 2-D MESFET technology into the large scale IC manufacturing environment.

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